

(51) International Patent Classification <sup>6</sup> : <b>H01L</b>		<b>A2</b>	(11) International Publication Number: <b>WO 97/28558</b>
			(43) International Publication Date: 7 August 1997 (07.08.97)
(21) International Application Number: <b>PCT/US97/00927</b>		(74) Agent: HARRIS, Scott, C.; Fish & Richardson P.C., Suite 1400, 4225 Executive Square, La Jolla, CA 92037 (US).	
(22) International Filing Date: 22 January 1997 (22.01.97)			
(30) Priority Data:		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
60/010,305 22 January 1996 (22.01.96) US			
60/013,700 20 March 1996 (20.03.96) US			
(60) Parent Applications or Grants			
(63) Related by Continuation			
US 60/013,700 (CON)			
Filed on 20 March 1996 (20.03.96)			
US 60/010,305 (CON)			
Filed on 22 January 1996 (22.01.96)			
(71) Applicant (for all designated States except US): CALIFORNIA INSTITUTE OF TECHNOLOGY [US/US]; 1201 East California Boulevard, Pasadena, CA 91125 (US).		<b>Published</b> Without international search report and to be republished upon receipt of that report.	
(72) Inventor; and			
(75) Inventor/Applicant (for US only): FOSSUM, Eric, R. [US/US]; Photobit, Suite 104, 2529 Foothill Boulevard, La Crescenta, CA 91214 (US).			

The diagram illustrates a memory array architecture. On the left, a **ROW-DECODER** (1022) is connected to a **MIX** block (1024). The MIX block outputs four row signals:  $\phi G1$ ,  $\phi G2$ ,  $\phi G3$ , and  $\phi G4$ . These signals are connected to a 4x4 array of access transistors (1020). Each access transistor is represented by a square symbol. The array is connected to a sense amplifier (1028) which includes a cross-coupled pair of transistors (1032, 1034) and a feedback loop (1036, 1038). The sense amplifier is connected to a **NSC** (Not Sense Control) block (1040) which outputs a signal  $\phi_{NSC}$ . The array is also connected to a **COL-DECODER** (1024) which outputs a signal  $\phi_{COL}$ . The array is connected to a sense amplifier (1028) which includes a cross-coupled pair of transistors (1032, 1034) and a feedback loop (1036, 1038). The sense amplifier is connected to a **NSC** (Not Sense Control) block (1040) which outputs a signal  $\phi_{NSC}$ . The array is also connected to a **COL-DECODER** (1024) which outputs a signal  $\phi_{COL}$ .

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgyzstan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	KZ	Kazakhstan	SG	Singapore
CH	Switzerland	LI	Liechtenstein	SI	Slovenia
CI	Côte d'Ivoire	LK	Sri Lanka	SK	Slovakia
CM	Cameroon	LR	Liberia	SN	Senegal
CN	China	LT	Lithuania	SZ	Swaziland
CS	Czechoslovakia	LU	Luxembourg	TD	Chad
CZ	Czech Republic	LV	Latvia	TG	Togo
DE	Germany	MC	Monaco	TJ	Tajikistan
DK	Denmark	MD	Republic of Moldova	TT	Trinidad and Tobago
EE	Estonia	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	UG	Uganda
FI	Finland	MN	Mongolia	US	United States of America
FR	France	MR	Mauritania	UZ	Uzbekistan
GA	Gabon			VN	Viet Nam

**ACTIVE PIXEL SENSOR ARRAY WITH ELECTRONIC SHUTTERING**Origin of the Invention:

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

Related Applications:

This application is a continuation-in-part of U.S. patent application Serial No. 08/558,521, which is a continuation of 08/188,032 filed January 28, 1994 entitled ACTIVE PIXEL SENSOR WITH INTRA-PIXEL CHARGE TRANSFER by Eric R. Fossum et al. and assigned to the present assignee. This application also claims priority from provisional application number 60/010,305, filed January 22, 1996, and from provisional application number 60/013,700, filed March 20, 1996.

Field of the invention:

The invention is related to semiconductor imaging devices. More specifically, the present invention relates to a silicon imaging device which can be fabricated using a

CMOS compatible process, and specific improved techniques that are used by such a system.

Background and Summary:

Many semiconductors can be used for acquiring a signal indicative of an image. Charge coupled devices (CCDs), photodiode arrays, charge injection devices and hybrid focal plane arrays are some of the more commonly used devices. CCDs are often used, since they represent a mature technology, are capable of large formats and very small pixel size and they facilitate noise-reduced charge domain processing techniques such as binning and time delay integration.

However, CCD imagers suffer from a number of drawbacks. For example, the signal fidelity of a CCD decreases as the charge transfer efficiency is raised to the power of the number of stages. Since CCDs use many stages, the CCD fabrication technique needs to be optimized for very efficient charge transfer efficiency. CCDs are also susceptible to radiation damage, require good light shielding to avoid smear and have high power dissipation for large arrays.

The specialized CCD semiconductor fabrication process is intended to maximize the charge transfer efficiency of the CCD. This specialized CCD process, however, has been

incompatible with the complementary metal oxide semiconductor ("CMOS") processing which has been conventionally used. The image signal processing electronics required for the imager are often fabricated in CMOS. Accordingly, it has been difficult to integrate on-chip signal processing electronics in a CCD imager, because of the incompatibility of the processing techniques. Because of this problem, the signal processing electronics has often been carried out off-chip.

Typically, each column of CCD pixels is transferred to a corresponding cell of a serial output register, whose output is amplified by a single on-chip amplifier (e.g., a source follower transistor) before being processed in off-chip signal processing electronics. This architecture limits the read-out frame rate which the on-chip amplifier can handle proportional to the number of charge packets divided by the number of pixels in the imager.

The other types of imager devices have problems as well. Photodiode arrays exhibit high kTC noise. The kTC noise makes it impractical to reset a diode or capacitor node to the same initial voltage at the beginning of each integration period. Photodiode arrays also suffer from lag. Charge injection devices also have high noise.

Hybrid focal plane arrays exhibit less noise but are prohibitively expensive for many applications and have relatively small array sizes.

5 In view of the inventors recognition of the above problems, it is one object of the present invention to provide an imager device which has the low kTC noise level of a CCD without the associated CMOS incompatibility and other above-described problems.

10 In addition, there is a need in imaging devices to control the integration or exposure time of the sensor. This control allows decreasing the integration time for imaging relatively bright objects to avoid saturating the pixels. Conversely, it is sometimes desirable to increase the integration time to increase the resolution of  
15 relatively dim objects.

Control of the integration time is also advantageous in video imaging applications where it is desired that this period be less than the inverse of the frame rate. Thus, if the integration period is  $T$  and the frame rate is  $f$ , it is  
20 desirable that  $T \leq 1/f$ .

Integration time has been controlled in the past with mechanical shutters. However, the mechanical nature of these devices made the shuttering imprecise. This caused the integration time to vary significantly. In addition,  
25 once configured, the mechanical-type shutters could not

easily be adjusted, for example, to shutter a different portion of the array or to change adaptively. A controllable electronic shutter in each pixel cell would provide a more efficient, precise, and versatile way of setting the integration time of the array or a part of the array.

Furthermore, it is advantageous in some applications that some or all the pixels be integrated simultaneously for the same absolute period of time. This simultaneous integration prevents motion skew in the image by providing a "stop-action" or "snap shot" image. The alternative to simultaneous integration is to accumulate charge in only a portion of the pixel cells being employed to image an observed scene. For example, an imaging system might operate by scanning a row of the array at a time to produce an overall image. Thus, the resultant image has a series of lines, each of which represents a part of the observed scene at a different time. Obviously, if the scene is changing quickly enough, the image will be skewed as stated above.

Therefore, this piecemeal method of creating an image would be inappropriate for certain quickly changing scenes. However, by integrating all the pixels in the array simultaneously and capturing the accumulated charge, a "snap shot" of the scene encompassing the period of integration can be obtained. The captured accumulated charge would then

be readout and processed in some sequential method to create the desired image.

In view of the above, one aspect of the present invention is embodied in an imaging device formed as a monolithic complementary metal oxide semiconductor integrated circuit in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photosensing element, e.g., a photogate, overlying the substrate for accumulating photo-generated charge in an underlying portion of the substrate and a charge coupled device section formed on the substrate adjacent the photogate having a sensing node and at least one charge coupled device stage for transferring charge from the underlying portion of the substrate to the sensing node.

In a preferred embodiment, the sensing node of the charge coupled device section includes a floating element -- e.g., a diffusion, and the charge coupled device stage includes a transfer gate overlying the substrate between the floating diffusion and the photogate. This preferred embodiment can further include apparatus for periodically resetting a potential of the sensing node to a predetermined potential, including a drain diffusion connected to a drain bias voltage and a reset gate between the floating diffusion



and the drain diffusion, the reset gate connected to a reset control signal.

The imaging device also includes a readout circuit having at least an output transistor. Preferably, the output transistor is a field effect source follower output transistor formed in each one of the pixel cells, the floating diffusion being connected to its gate. Also, the readout circuit can further include a field effect load transistor connected to the source follower output transistor, and preferably a correlated double sampling circuit having an input node connected between the source follower output transistor and load transistor. The focal array of cells is also preferably organized by rows and columns, and the readout circuit has plural load transistors and plural correlated double sampling circuits. In this case, each cell in each column of cells is connected to a single common load transistor and a single common correlated double sampling circuit. These common load transistors and correlated double sampling circuits are disposed at the bottom of the respective columns of cells to which they are connected.

In the preferred implementation, charge is first accumulated under the photogate of a pixel cell. Next, the correlated double sampling circuit samples the floating diffusion after it has been reset. The accumulated charge

is then transferred to the floating diffusion and the sampling process is repeated with the result stored at another capacitor. The difference between the two stored values represents the signal output. In accordance with a further refinement, this difference is corrected for fixed pattern noise by subtracting from it another difference sensed between the two values while they are temporarily shorted.

The imaging device can also have a micro-lens layer overlying the substrate. This micro-lens layer includes a refractive layer and individual lenses formed in the layer which are in registration with individual ones of the cells. Each of the individual lenses has a curvature for focusing light toward a photosensitive portion of the respective cell.

In addition, the imaging device can further include an electronic shutter formed on the substrate adjacent the photogate. This electronic shutter is capable of draining charge from the portion of the substrate underlying the photogate, thus preventing any accumulation thereof. Accordingly, when the electronic shutter is "closed" such that charge is being drained from the portion of the substrate under the photogate, the pixel cell is essentially deactivated. When the electronic shutter is in an "open"

mode, charge is allowed to accumulate under the photogate and the cell operates as described above.

The electronic shutter is preferably set in the "open" mode such that whenever charge accumulates under the photogate to a predetermined maximum level, any excess drains into a special sink in the electronic shutter, rather than into the floating diffusion. In this way, the electronic shutter provides a way to control the integration period of the cell, as well as lateral anti-blooming.

In addition to the just-described benefits, other objectives and advantages of the present invention will become apparent from the detailed description which follows hereinafter when taken in conjunction with the drawing accompanying figures.

#### BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will now be described in detail with reference to the accompanying drawings, wherein:

FIG. 1 is a diagram illustrating the architecture of a preferred individual focal plane cell;

FIG. 2 is a plan view of an integrated circuit having a focal plane array of cells of the type illustrated in FIG.

1.

FIG. 3A is a schematic diagram of the cell of FIG. 1.

FIG. 3B is a plan view of an integrated circuit constituting a focal plane array of cells of a type similar to FIG. 1, showing the load FET and sampling circuit as common elements at the bottom of each array column.

5        FIG. 4 is a graph of the surface potential in the charge transfer section of the cell of FIG. 3A;

FIG. 5 is a cross-sectional view of an alternative embodiment of the focal plane array of FIG. 2 including a micro-lens layer.

10       FIG. 6A shows a polymer filter embodiment;

FIG. 6B shows a multiple chip, separate color embodiment;

FIG. 6C shows a phosphor converting embodiment;

15       FIG. 6 is a schematic diagram of an alternate embodiment of the cell of FIG. 3A with a storage well and an additional charge coupled device stage, and includes a graph of the surface potential in the charge transfer section.

20       FIG. 7 is a schematic diagram of an alternate embodiment of the cell of FIG. 3A with an electronic shutter and overlapping photogate, including a graph of the surface potential in the charge transfer section; and

FIG. 8 is a schematic diagram and surface potential graph of the embodiment of FIG. 7 without the overlapping photogate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a simplified block diagram of one pixel cell 10 of a focal plane array of many such cells formed in an integrated circuit. Each cell 10 includes a photogate 12, a charge transfer section 14 adjacent the photogate 12 and a readout circuit 16 adjacent the charge transfer section 14. FIG. 1 shows these elements with the square area being labelled the pixel, but it should be understood that these elements can alternatively be physically located outside the area called the pixel.

FIG. 2 shows a focal plane array of many cells 10 formed on a silicon substrate 20.

FIG. 3A is a simplified schematic diagram of a cell 10 and its associated processing. Each pixel 300 includes a photogate area and its associated circuitry (30 - 50) and row decoder elements 55, 60. FIG. 3A shows the photogate 12 having a relatively large photogate electrode 30 overlying the substrate. The charge transfer section 14 has a transfer gate electrode 35 adjacent the photogate electrode 30, a floating diffusion 40, a reset electrode 45 and a drain diffusion 50. The readout circuit 16 has a source follower field effect transistor (FET) 55, a row select FET 60, a load FET 65 and a correlated double sampling circuit 70.

The surface potential diagram of FIG. 4 shows the photogate electrode 30 being held by a photogate signal PG at a positive voltage to form a potential well 80 in the substrate 20 in which photo-generated charge is accumulated during an integration period. The transfer gate electrode 35 is initially held at a less positive voltage by a transfer gate signal TX to form a potential barrier 85 adjacent the potential well 80. The floating diffusion 40 is connected to the gate of the source follower FET 55 whose drain is connected to a drain supply voltage VDD. The reset electrode 45 is initially held by a reset signal RST at a voltage corresponding to the voltage on the transfer gate 30 to form a potential barrier 90 thereunder. The drain supply voltage VDD connected to the drain diffusion 50 creates a constant potential well 95 underneath the drain diffusion 50.

During the integration period, electrons accumulate in the potential well 80 in proportion to photon flux incident on the substrate 20 beneath the photogate electrode 30. At the end of the integration period, the surface potential beneath the floating diffusion 40 is quickly reset to a potential level 100 slightly above the potential well 95. This is accomplished by the reset signal RST temporarily increasing to a higher positive voltage to temporarily remove the potential barrier 90 and provide a downward

potential staircase from the transfer gate potential barrier 85 to the drain diffusion potential well 95, as indicated in the drawing of FIG. 4. After the reset gate 45 is returned to its initial potential (restoring the potential barrier 90), the readout circuit 70 briefly samples the potential of the floating diffusion 40, and then the cell 10 is ready to transfer the photo-generated charge from beneath the photogate electrode 30. For this purpose, the photogate signal PG decreases to a less positive voltage to form a potential barrier 105 beneath the photogate electrode 30 and thereby provide a downward staircase surface potential from the photogate electrode 30 to the potential well 100 beneath the floating diffusion 40. This operation transfers the charge from beneath the photogate electrode 30 to the floating diffusion 40, changing the potential of the floating diffusion 40 from the level (100) at which it was previously reset to a new level 107 indicative of the amount of charge accumulated during the integration period. This new potential of the floating diffusion 40 is sensed at the source of the source follower FET 55. However, before the readout circuit 70 samples the source of the source follower FET 55, the photogate signal PG returns to its initial (more positive) voltage. The entire process is repeated for the next integration period.

The readout circuit 70 has a signal sample and hold (S/H) circuit including an S/H FET 200 and a signal store capacitor 205 connected through the S/H FET 200 and through the row select FET 60 to the source of the source follower FET 55. The other side of the capacitor 205 is connected to a source bias voltage VSS. The one side of the capacitor 205 is also connected to the gate of an output FET 210. The drain of the output FET is a connected through a column select FET 220 to a signal sample output node VOUTS and through a load FET 215 to the drain voltage VDD. A signal called "signal sample and hold" (SHS) briefly turns on the S/H FET 200 after the charge accumulated beneath the photogate electrode 30 has been transferred to the floating diffusion 40, so that the capacitor 205 stores the source voltage of the source follower FET 55 indicating the amount of charge previously accumulated beneath the photogate electrode 30.

The readout circuit 70 also has a reset sample and hold (S/H) circuit including an S/H FET 225 and a signal store capacitor 230 connected through the S/H FET 225 and through the row select FET 60 to the source of the source follower FET 55. The other side of the capacitor 230 is connected to the source bias voltage VSS. The one side of the capacitor 230 is also connected to the gate of an output FET 240. The drain of the output FET 240 is connected through a column



select FET 245 to a reset sample output node VOUTR and through a load FET 235 to the drain voltage VDD. A signal called "reset sample and hold" (SHR) briefly turns on the S/H FET 225 immediately after the reset signal RST has  
5 caused the resetting of the potential of the floating diffusion 40, so that the capacitor 230 stores the voltage to which the floating diffusion has been reset.

The readout circuit provides a special form of correlated double sampling of the potential of the floating  
10 diffusion, allowing the charge integrated beneath the photogate 12 during each integration period to be obtained at the end of each integration period from the difference between the voltages at the output nodes VOUTS and VOUTR of the readout circuit 70. This minimizes the effects of kTC  
15 noise because the difference between VOUTS and VOUTR is independent of any variation in the reset voltage on the floating diffusion 40. It also suppresses fixed pattern noise produced by threshold variations in transistor 55. It also suppresses 1/F noise produced by transistors 55, 60 and  
20 65.

FIG. 5 shows a transparent refractive microlens layer 110 which may be deposited over the top of the focal plane array of FIG. 2. The microlens layer 110 has spherical portions 115 centered over each of the cells 10 and  
25 contoured so as to focus light toward the center of each

photogate 12. This has the advantage of using light that would otherwise fall outside of the optically active region of the photogate 12. For example, at least some of the light that is ordinarily incident on either the charge transfer section 14 or the readout circuit 16 (FIG. 1) would be sensed in the photogate area with the addition of the microlens layer 110. This has the effect of maximizing real estate - the portions of the substrate which include the non-photogate area are focused to another point.

FIG.s 6A and 6B show an alternative embodiment of the invention which uses color filtering. Color filtering enables spatial separation of color in an imaging device. CCD devices, for example, commonly use kind of color separation in this way.

The preferred system allows a plurality of pixels to have different color filtering properties to provide a color filtering effect. Typically this is done by using the color filters in some array form: For example, alternate green filters interspersed with red and blue filters. An exemplary filter operation would use green/red/green/blue/green/red/green/blue with that pattern continuing for the length of the array.

According to this embodiment of the present invention, color filters are used to supplement the lens operation of FIG. 5.

5 The preferred system embodies its operation in one of the two forms shown in FIG.s 6A and 6B. The first form shown in FIG. 6A uses a polymer color filter array. Such polymer color filter arrays are well-known in the art. Layer 600 is preferably a red layer, and is first deposited over the entire chip. Subsequent to deposition, an etching  
10 technique is used to remove the red filter area 600 from everywhere except over the desired pixel 10. A planarization layer 602 covers the removed areas to thereby planarize that surface, thereby flattening the surface. Blue filter 604 is next deposited over pixel 10A. Blue  
15 filter 604 is similarly etched such that it only covers the desired pixel 10A. The remaining area is planarized by a second planarization layer 606. Finally, a green filter 610 is formed over that planarized layer, covering pixel 10B. Planarization layer 612 flattens the resulting area so that  
20 green filter 610 only covers the pixel 10B.

Each pixel, including the polymer layer, is covered by microlens 115A; 115B and 115C. The microlenses modify the incoming light in conjunction with the polymer layer. The light is therefore changed by both microlenses 115A-115C and  
25 CFA parts 612, 606, and 600. Each pixel, therefore,

preferably receives light that has been altered by the lens and altered by the color filter array.

This polymer color filter array sacrifices a certain amount of resolution of the scene. Each pixel of the scene is imaged by three pixels, and hence some of the pixels are dedicated to a different color.

An alternative embodiment shown in FIG. 6B does not lose resolution, but instead requires multiple chips to form any image. This would form a 3-chip camera. One chip has all its pixels covered by a red filter. Hence that chip images the red scene - either the red components or the complement to the red components. Analogously, the other chips include green filters and blue filters. The three chips together form the entire image.

Yet another embodiment uses a wavelength-converting phosphor as shown in FIG. 6C. A wavelength-converting phosphor is typically tuned to accept radiation of a desired wavelength, e.g., ultra-violet or x-ray. Typically the silicon underlayer is not responsive to that same wavelength. Therefore, the phosphor emits a photon of the proper type to properly excite the underlying silicon, when receiving this radiation. A preferred example is that the phosphor is sensitive to x-ray, but emits a photon of green light that is detected by the circuitry which can be a sensor of any of the kinds described herein.

While the FIG. 6C embodiment contemplates using the wavelength-converting phosphor over an entire surface of the device, it is also possible to use a pixelation effect. A shadow mask is used to mask the phosphor. The phosphor is only deposited where allowed by the shadow mask.

It should also be understood that these same techniques could be embodied in other focal plane and photodiode applications, and that the above color filter array is not limited to single readout circuit per pixel systems.

Preferably, the focal plane array corresponding to FIG.s 1-4 is implemented in MOS silicon or CMOS, or any other technology which is compatible with an industry standard CMOS fabrication process. Preferably, each of the FETs is a MOSFET, the FETs 55, 60, 65, 200 and 225 being n-channel devices and the FETs 210, 220, 225, 230, 240, 245 being p-channel devices. The n-channel MOSFETS and the CCD channel underlying the gate electrodes 30, 35, 45 and the diffusions 40 and 50 may be located in a p-well while the remaining (p-channel) devices are located outside of the p-well. The gate voltage VLP applied to the gates of the p-channel load FETs 215 and 235 is a constant voltage on the order of +2.5 volts. The gate voltage VLN applied to the n-channel load FET 65 is a constant voltage on the order of +1.5 volts.

The charge transfer section 14 preferably uses only a single CCD stage between the photogate 12 and the floating diffusion 40 in the specific embodiment of FIG. 3A. This means that there is no loss due to charge transfer

5 inefficiency and therefore there is no need to fabricate the device with a special CCD process. As a result, the readout circuit 70 as well as the output circuitry of the FETs 55, 60 and 65 can be readily implemented as standard CMOS circuits, making them relatively inexpensive. However, any  
10 suitable charge coupled device architecture may be employed to implement the charge transfer section 14, including a CCD having more than one stage. For example, two or three stages may be useful for buffering two or three integration periods.

15 Other implementations of the concept of the invention may be readily constructed by the skilled worker in light of the foregoing disclosure. For example, the floating diffusion 40 may instead be a floating gate electrode. The signal and reset sample and hold circuits of the readout  
20 circuit 70 may be any suitable sample and hold circuits. Moreover, shielding of the type well-known in the art may be employed defining an aperture surrounding the photogate 12. Also, the invention may be implemented as a buried channel, n-well, or p-channel device.

Another feature of the invention which is useful for eliminating fixed pattern noise due to variations in FET threshold voltage across the substrate 20 is a shorting FET 116 across the sampling capacitors 205, 235. After the accumulated charge has been measured as the potential difference between the two output nodes VOUTS and VOUTR, a shorting signal VM is temporarily applied to the gate of the shorting FET 116 and the VOUTS-to-VOUTR difference is measured again. This latter difference is a measure of the disparity between the threshold voltages of the output FETs 210, 240, and may be referred to as the fixed pattern difference. The fixed pattern difference is subtracted from the difference between VOUTS and VOUTR measured at the end of the integration period, to remove fixed pattern noise.

As previously mentioned herein, a floating gate may be used instead of the floating diffusion 40. Such a floating gate is indicated schematically in FIG. 3A by a simplified dashed line floating gate electrode 41.

In one preferred implementation, the area of the photogate 12 (i.e., the photogate electrode 30) is preferably L-shaped as shown in FIG. 1, and is about 100 square microns; the transfer gate electrode 35 and the reset gate electrode were each about 1.5 microns by about 6 microns; the photogate signal PG was varied between about +5 volts (its more positive voltage) and about 0 volts (its less positive

voltage; the transfer gate signal TX was about +2.5 volts; the reset signal RST was varied between about +5 volts (its more positive voltage) and about +2.5 volts (its less positive voltage); the drain diffusion 50 was held at about +5 volts.

The array structure of FIG.s 1-4 can be modified to incorporate a preferred column parallel approach. The term column parallel approach refers to a portion of the readout circuitry being connected to the bottom on the columns of the array. This allows an entire row of the array to be processed at one time. This column approach is in contrast to a spatially parallel processing approach where each pixel has its own processing circuitry (e.g., the embodiment of FIG.s 1-4), or a serial processing approach where the output of each pixel is sequentially feed to a single processor for processing.

FIG. 3B shows a column parallel approach where the load FET 65 and correlated double sampling circuit 70 are deleted from the individual pixel cells 10. Instead, each cell 10 in a column of the array is connected to a common load FET 65 and sampling circuit 70. The common elements are preferably located at the bottom of each column of the array. This column parallel array structure has a significant advantage. Since the load FET 65 and sampling circuit 70 have been removed from the pixel cells 10, there



is more photosensitive cell area available. Thus, the resolution of each cell 10 is improved. The column parallel array structure is read out by selecting an entire row using standard row and column select circuitry 18, 19. Selecting a row, among other things, results in the accumulated charge being transferred from the photogate potential well 80 of each cell 10 in the row to its associated floating diffusion 40. Thereafter, the sampling circuits 70 at the bottom of each column "read" the connected pixel cell 10 in the manner described previously. A standard multiplexer 21 is then employed to output the "read" pixel cell values, either in parallel or serially.

The previous described pixel cell structure of FIG.s 3A or 3B and 4 can be further modified to include simultaneous integration of the array. In the originally-described pixel cell structure, charge accumulated in the photogate well 80 during the integration period was transferred directly to the floating diffusion 40. However, in many applications, not all the cells in the array could be read out at the same time. The charge that was transferred to the floating diffusion 40 would degrade over time.

One counter measure to this problem is to transfer only the accumulated charge for pixel cells that are currently being read out. For example, as described in connection with the embodiment of fig. 3B, only a row of the array is

read out at one time. However, since only a portion of the array is read out, the resulting image from all the cells represents a series of lines, each corresponding to the observed scene at a different time. If the observed scene is changing, the resulting image may be motion-skewed, i.e., may have some portions that represent a different instant of time than others. At the same time, it is important that noise be minimized.

FIG. 6 shows an embodiment that accomplishes these goals according to the technique of the present invention, by incorporating additional structure into the basic cell structure. A storage gate electrode 260 overlies a storage potential well 265 in the substrate. The storage well 265 is a supplemental charge storage area which stores charge from the main light collection area -- photogate well 80. The size of storage well 265 depends on the necessary charge amount. In low light situations, for example, the area of the optical charge storage area may need to be large in order to collect as much light as possible. However, the charge storage area may never fill. In that case, storage well needs only enough area to store the intended amount of charge. For maximum light-collection capability, however, storage well 265 preferably has a similar surface area as the photogate well 80 to ensure that all the charge

accumulated in the photogate well 80 can be transferred to the storage well 265.

The non-photosensitive portion of the pixel cell is preferably shielded from optical radiation by an opaque layer 270, e.g., a metal layer. The non-photosensitive portion of the cell includes the area underlying the intermediate transfer gate 255 and storage gate 260, as well as the transfer gate 35, floating diffusion 40, reset gate 45, and  $V +$  drain 50.

This optical shielding layer 270 minimizes the possibility that optically generated noise affects the charge stored in the storage well 265, or the other identified structures.

The process for operating this modified pixel cell is similar to that described previously. A control system 600 supplies voltage. The charge accumulated in the photogate well 80 under the photogate electrode 30 during the integration period is then transferred across the intermediate transfer gate 255 and into the storage potential well 265. The charge remains in well 265 until readout. The voltage  $VP_g$  on the photogate electrode 30 is initially greater than the voltage  $VT_g$  of intermediate transfer gate 255. When the image acquisition is complete,  $VP_g$  is reduced to less than  $VT_g$ . This forms potential barrier 105 beneath the photogate electrode 30, thereby

providing a downward staircase surface potential from the photogate electrode 30 to the storage well 265 which is being held at a higher positive voltage than the intermediate transfer gate 255. During readout, the floating diffusion node 40 is reset and the reset voltage sampled, as discussed previously. At the time of the readout, the charge is transferred from the storage well 265 over the transfer gate potential 85 and into the floating diffusion node 40, where it is sampled, in the same way the charge was transferred from the photogate well 80 to the node 40 in the first-described embodiment of FIG.s 3A-B and 4.

The techniques of the storage well 265 and transferring of the charge from the photogate well 80 to the storage well 265 after the integration period enables simultaneous integration. The accumulated charge in each cell is transferred to its associated storage well 265 at the end of the integration period. Therefore, all the pixel cells, or a part as desired, can be used to image the observed scene for the duration of the prescribed integration period, regardless of when each individual cell is to be read out. This allows a "snapshot" image to be stored.

The storage well 265 provides a stable structure in which to store the transferred charge. However, an important part of the present invention is the ability to

store shuttered information in a way that still allows correlated double sampling.

Different techniques of double sampling are well known in the art. The inventors of the present invention, however, desire to obtain the most possible accuracy. This requires determining the amount of incoming flux with errors that are within the single electron range. The inventors recognize that because of quantum imperfections and fluctuations, it is not possible to obtain certainty about a reset level unless that reset level is actually monitored, each time at the beginning of the cycle. Some previous systems have correlated the reset that occurs at the end of one cycle with the full value at the end of the next cycle. This provides, on the average, a good approximation of the value. However, since we can never be precisely sure of the exact value which is present at the beginning and end of a cycle, this system allows less accuracy than the present invention. This embodiment, allow the flowing diffusion to be monitored prior to the introduction of charge thereto. In this way, the system of the present invention enables a more accurate detection than that which has been available previously. Moreover, and the accumulated and transferred charge can remain in the storage well 265, preferably substantially isolated from noise or leakage, until the time of readout for that cell. The charge is transferred to the

floating diffusion 40. The above-described technique ensure there is minimal degradation of the signal produced even though the charge was stored for some period of time, an improved detection values.

5           This simultaneous integration pixel cell structure trades off the ability to store a snapshot against the fill factor of the cell. The intermediate transfer gate 255 and storage gate 260 take up room on the substrate and are shielded from optical radiation. Therefore, the proportion  
10 of the cell that is actively photosensitive is reduced. This may have the effect of lowering the resolution of the cell for any particular cell size.

          A certain amount of this real estate can be reclaimed using the technique shown in FIG. 6A. FIG. 6A shows one  
15 particular pixel, including a photosensitive part 610, and a non-photosensitive part 612. As described in the preferred embodiment, the non-photosensitive part 612 is covered by blocking layer 270. Planarization layer 614, preferably an opaque layer which does not affect the optical radiation  
20 passing therethrough, covers the photosensitive portion 610. This forms a flat surface 616.

          As in previous embodiments, a color filter 618 is optionally formed over the planarized layer including the optical blocking layer and the planarization layer. FIG. 6A  
25 shows the color filter formed over the entire pixel, but it

should be understood that the color filter need not cover the entire pixel since part of this is blocked.

The entire structure is covered by lens 620, which is formed to refract light incoming from over the non-photosensitive area 612 towards the photosensitive area 610. This lens can recapture some of the light which would otherwise fall on the shielded area and refract it to increase some of the resolution.

Another embodiment of the active pixel sensor array allow control over the length of the integration period using alternate electronic shutter shown in FIG. 7. Shutter gate 302 and a shutter drain diffusion 304 are positioned relative to the photogate 30 to bleed off charge away from the photogate. Although shown as a separate elements in FIG. 7, in practice the shutter drain diffusion 304 may also act as the previously described V+ drain 50, either for the same pixel or of an adjacent pixel in the array. In either case, the shutter drain diffusion 304 is maintained at a positive voltage exceeding the potential of the other gates to form a potential well shown as 300 under drain diffusion 304.

The shutter gate 302 and shutter drain diffusion 304 act together to selectively prevent charge accumulation in the associated pixel or allow the accumulation of an optically generated charge under the photogate 30 when

desired. Accumulation of charge is prevented by biasing shutter gate 302 to a positive voltage which exceeds the bias on the photogate 30. This forms a potential barrier 306. At the same time the bias on the transfer gate 35 is made less than that on the photogate electrode 30 to form potential barrier 308. This creates a downward staircase in surface potential from the photogate electrode 30 via well 306 to the potential well 300 beneath the shutter drain diffusion 304. This downward staircase allows any optically generated charge in the photogate potential well 80 spills across the shutter gate 302 into potential well 300 and into shutter drain diffusion 304. In this mode, the electronic shutter is effectively "closed" since optically generated charge is not allowed to accumulate.

To begin the accumulation of charge in the photogate potential well 80, the shutter gate bias is changed to a voltage lower than the photogate 30, but slightly higher than the transfer gate 35. This forms potential barrier 310. The inventors prefer making the shutter gate bias slightly higher than that of the transfer gate 35. In the case of a very strong optical signal, the photogate potential well 80 fills until charge begins to flow over the shutter gate potential 310 into the shutter drain diffusion 304. Therefore, charge does not leak past the transfer gate potential 308 and into the floating diffusion node 40 where



it could disrupt the readout process described earlier. This specific expedient allows a lateral anti-blooming control in the pixel cell and provides an additional advantage to the electronic shutter structure.

5           At the end of a selected integration period, the charge accumulated under the photogate 30 is shifted to the floating diffusion node 40 (or storage well) by lowering the shutter gate bias to a voltage below the bias voltage of the transfer gate 35 to form potential barrier 312, and then  
10           pulsing the photogate bias to a similar lower voltage to form potential barrier 314. This causes the charge accumulated during the selected integration period to flow over the transfer gate potential 308 and into the floating diffusion node 40. After the transfer of charge, the  
15           electronic shutter can be closed once again, or a new integration cycle can be initiated by adjusting the shutter gate and photogate biases as described above.

          The section of the pixel cell from the diffusion node 40 side edge of the photogate 30, through the transfer gate  
20           35, floating diffusion node 40, reset gate 45, and V+ drain 50 is preferably covered with an opaque layer 316, such as one made of metal, to block optical radiation and reduce optically-generated noise in the underlying substrate.

          In a preferred implementation of the electronic  
25           shutter, the shutter gate 302 is biased to the V+ drain

potential (i.e., about 5 volts), the photogate 30 is biased to about 4 volts, and the transfer gate 35 is biased to about 1.2 volts, in the "closed" mode. To initiate the integration mode (i.e., "open" the shutter), the shutter gate potential is changed to about 1.5 volts, while the other gate potentials remain the same. The accumulated charge is transferred to the floating diffusion node 40, by setting the shutter gate 302 at 0 volts and the photogate 30 is pulsed to this same potential.

The electronic shutter makes it possible to set a desired integration time for all or some of the cells. The integration time for any one cell is set by simply "opening" the electronic shutter for a predetermined period of time.

The pixel cell in FIG. 7 uses overlapping gates 318. The photogate 30 overlaps the shutter gate 302, and transfer gate 35, over the surface of the pixel cell substrate. This overlapping gate structure enhances the charge transfer efficiency discussed previously. This enhancement results from reducing the area of the substrate that would otherwise have to exist between adjacent gates. This area is placed under the influence of one of the gate potentials. Accordingly, the charge transfer is facilitated. However, there is a tradeoff. The formation of overlapping gates 318 in a CMOS device requires a double poly process. Advanced CMOS fabrication processes which use only a single layer of

poly can be used. Therefore, spaced gates with intervening gaps are a necessity in these single poly layer CMOS implementations. In such a structure, floating diffusions 320 are created in the substrate under the gaps 322 between the photogate 30, shutter gate 302, and the transfer gate 35, as shown in FIG. 8.

Any overlap described herein can be replaced a floating diffusion with non-overlapping poly from a single poly layer.

Although only a few embodiments have been described in detail above, those having ordinary skill in the art will certainly understand that many modifications are possible in the preferred embodiment without departing from the teachings thereof.

All such modifications are intended to be encompassed within the following claims.

What is claimed is:

1. An optical device, comprising:

5 a light collection area, comprising a photogate  
and an optical storage area which is controlled by said  
photogate, said optical storage area operating to accumulate  
optical charge under control of said photogate;

a supplemental charge storage area, physically  
separated from said light collection area;

10 a charge transfer mechanism, coupled between said  
light collection area and said charge storage area, said  
charge transfer mechanism comprising an operable device  
which is selectively operable to transfer charge in said  
light collection area to said supplemental charge storage  
15 collection area; and

an output node, connected to receive charge from  
said supplemental charge storage area, and including a  
control element which transfers charge from said light  
collection area to said output node, said output node being  
20 electrically floated when unconnected.

2. A device as in claim 1 wherein said light  
collection area has a first area, said supplemental charge  
storage area has a second area smaller than said first area.

25

3. A device as in claim 1 wherein said light collection area has a first area, said supplemental charge storage area has a second area that is substantially the same as said first area.

5

4. A device as in claim 1 further comprising a control element, said control element provides a potential on the photogate which is initially lower than a potential on the charge transfer mechanism to allow charge to be accumulated therein.

10

5. A device as in claim 1 wherein said output node comprises a floating node, a first element, operating to sample a voltage on the floating node prior to transfer of charge thereto, and a second element operating to sample a voltage on the floating node after transfer of charge thereto.

15

6. A device as in claim 1, further comprising an optical shield, optically covering at least a portion of the supplemental charge storage area.

20

7. A device as in claim 6 further comprising a microlens overlying the optical shield, and refracting at

least a portion of the light impinging over an area of the optical shield to the light collection area.

8. An optical pixel cell device comprising:

5 a substrate, having an optical blocking layer located adjacent said substrate, dividing said substrate into an optically blocked area, and an optically unblocked area;

10 a charge accumulating device, located in said optically unblocked area; and

a charge storage device located in said optically blocked area.

15 9. A device as in claim 8 wherein said charge accumulating device includes a controlling gate, and further comprising a control device which biases a gate on the charge accumulating device to a first level which allows said charge accumulation device to collect light, and prevents said light from passing into said blocked area, and  
20 then to a second level which allows light to pass to said blocked area.

10. A device as in claim 8 further comprising a floating diffusion, and a transfer gate, connected to

transfer charge from said charge storage device to said floating diffusion.

11. A device as in claim 10, further comprising a charge sink, and an element for transferring charge in said charge accumulating device to said charge sink, said transferring element set at a potential which is lower than an off potential of the transfer gate to prevent blooming.

12. A device as in claim 8, further comprising a lens element layer, formed as a layer overlying at least a portion of said optically blocked layer, and which refracts light from said optically blocked layer to said optically unblocked layer.

13. An active pixel sensor system, comprising:  
a substrate with a light collection area including a light collecting photogate well and a photogate which selects whether said light collecting photogate well receives charge or not, dependent on a state of an applied voltage thereto;

a shutter element, which prevents accumulation of charge in said light collection area;

a floating sensing element, and a gate which selectively provides charge to said floating sensing element;

5 a control system, controlling said gates and said shutter element, such that a charge on said floating sensing element is sampled at a beginning of a first period of integration, and a charge on said floating sensing element is sampled at an end of the same first period of integration, and said shutter is turned on to prevent said  
10 accumulation of charge at least at one of said beginning and end of said first period; and

a circuit which correlates said beginning and said end samples to form a correlated measurement.

15 14. A sensor as in claim 13 further comprising a storage well and a storage transfer element, wherein a voltage is applying to said storage well at an end of an integration period to transfer charge from said photogate well to said storage well, and wherein charge is not  
20 transferred from said storage well to said floating element until after said beginning sample taken at said beginning of said first period of integration.



15. A sensor as in claim 14 further comprising an optical blocking element, covering at least said storage well.

5 16. An active pixel sensor with shuttering and correlated double sampling, comprising:

a photogate well including a photogate which controls application of charge into said photogate well, a charge shutter which selectively removes charge from said photogate when biased to a predetermined potential, a floating sampling point, a transfer gate which transfers charge from said photogate well to said floating sampling point, and a control circuit, controlling said transfer of charge, said control circuit also including a first sampling element which samples said floating sampling point at a beginning of a cycle, prior to transferring charge to said floating sampling point, and a second sampling element, which samples said floating sampling point at the end of a cycle, subsequent to transferring charge accumulated during a charge accumulation cycle.

10  
15  
20

17. An active pixel sensor as in claim 16 further comprising a storage well including a storage gate, and a second transfer gate, connecting said storage well to said photogate well, an output transfer gate connected to said

25

storage well, and wherein said control circuit controls said shutter to remain on during a time of charge collection, then to turn off, subsequently controls said second transfer gate to transfer charge from said photogate well to said charge storage well where it is stored therein, and subsequently, after said sampling at the beginning of the cycle, transferring said charge from said storage well to said floating gate.

18. An active pixel sensor as in claim 17 further comprising an optical light shielding layer, covering said storage well.

19. An active pixel sensor as in claim 16 wherein said shutter comprises a charge sink, and a charge sink transfer gate coupled between said photogate well and said charge sink, said transfer gate set at a first potential level to allow charge to accumulate in said photogate well and set at a second level to prevent charge from accumulating in said photogate well, and wherein a level of potential on said sink transfer gate being set to a level which is lower in potential than a level necessary to allow output to provide an anti-blooming control.

20. An active pixel sensor array, comprising:

a substrate having a plurality of chip areas, each said chip area defining a pixel, each said chip area including a photogate defining a collection area for a pixel, said collection area having an optically exposed surface which is exposed to incoming optical radiation, and each pixel area also including an optically shielded area that has an optical shield that shields it against incoming optical radiation, said optically-shielded area including circuitry which carries out a charge processing operation.

21. An array as in claim 20 wherein said optically shielded area includes a storage well for storing charge accumulated during a charge cycle, a transfer gate transferring charge that has accumulated to said optical storage well, a second light transfer mechanism, and a floating element, operating to receive charge from said second light transfer mechanism.

22. An array as in claim 21 further comprising an optical sink, and a sink transfer gate, selectively transferring charge to said optical sink;

said transfer gate biased to a level lower than a bias on said second light transfer mechanism.

23. An array as in claim 22, further comprising a floating node and sampling circuitry that samples a potential of said floating node prior to accumulation of charge, and again subsequent to said accumulation of charge.

5

24. A method of operating an active pixel sensor, comprising:

defining a beginning of an integration period and an end of an integration period during which integration period charge is to be accumulated;

10

accumulating charge in multiple photocollectors beginning at the beginning of the integration period to store incoming charge into a photogate well of multiple elements within the active pixel sensor;

15

at the end of the integration period, transferring accumulated charge from each said photocollector to an associated storage well;

sampling a value of first floating nodes;

20

transferring the charge from the storage well to said floating node at times that are subsequent to times when said first floating nodes are first sampled; and

25

after transferring the charge, sampling a value on said floating node again to obtain a correlated value indicating an amount of charge accumulated on the floating node.

25. A method as in claim 24 further comprising providing an anti-blooming control during the integration period.

5           26. A method as in claim 25 wherein said anti-blooming control comprises biasing a first gate which is connected to a sink to a level lower than said first level.

10           27. An active pixel sensor system with an electronic shutter, comprising:

          a photogate structure having a photogate well and a photogate element overlying said photogate well;

          a charge storage element, spaced from said photogate;

15           a shutter gate, connected between said photogate and said charge storage element, which is biased closed to prevent charge from accumulating in said photogate well, and is biased open to allow charge to accumulate in said photogate well, said shutter gate biased open to a level  
20           which avoids blooming.

          28. A system as in claim 27, further comprising an output gate, and wherein said output gate is biased closed during a time of charge accumulation, and said shutter gate  
25           is biased to a lower potential than a bias on said output

gate, so that excess charge spills into said shutter gate instead of said output gate and thereby prevents blooming.

29. A system as in claim 27 wherein said anti-blooming is formed by a charge sink and a charge transfer element, said charge transfer element biased to a level which causes extra charge to spill into said charge sink.

30. A system as in claim 29 wherein the shutter is closed by providing a first potential on the photogate and a second lower potential on the shutter gate connected to the photogate, such that all particles accumulated in the photogate spill over into the charge sink.

31. A system as in claim 30 wherein charge is accumulated in the photogate by raising a bias of the shutter to a potential which is higher than a potential of the potential well.

32. A system as in claim 30 further comprising an optical blocking element covering at least said shutter gate. wherein the third potential is higher than the potential well but not as high as the transfer gate to provide an anti-blooming control which limits an amount of

charge that can be collected and which prevents charge from leaking into the floating diffusion node.

33. A method of operating an active pixel sensor comprising:

accumulating charge by:

biasing a photogate well to a first potential level to allow charge to accumulate therein;

biasing an output gate, connected to said photogate well, to a second potential level higher than said first potential level to prevent charge from passing out of said photogate well via said output gate while charge is accumulating;

determining an amount of desired charge accumulation in said photogate; and

biasing a charge sink to a third potential level which is higher than said level of said photogate well by an amount related to said amount of desired charge accumulation, but lower than a level of bias of said output gate, to prevent charge accumulation beyond said desired amount from spilling past said output gate.

34. A method as in claim 33 further comprising providing a shutter operation by lowering said third potential level to a value less than the first potential in

said photogate well, thereby causing charge in said photogate well to spill into said charge sink.

35. An optical pixel cell device comprising:

5           a substrate, having an optical blocking layer located adjacent said substrate, dividing said substrate into an optically blocked area, and an optically unblocked area;

10           a charge accumulating device, having a charge accumulating controlling gate, located in said optically unblocked area;

          a charge storage device, having a charge storage controlling gate, located in said optically blocked area; and

15           a shuttering device, having a shuttering controlling gate, controlling shuttering of charge accumulating device;

          wherein at least one of said gates overlaps another of said gates over a surface of the substrate.

20           36. Apparatus as in claim 35 wherein said gates are formed by a double poly system.

37. An imaging device comprising:



a monolithic semiconductor integrated circuit substrate; and

a focal plane array of pixel cells, each of said pixel cells comprising:

5 a photogate, overlying said substrate, and capable of accumulating photo-generated charge in an underlying portion of said substrate,

a readout circuit,

10 a charge coupled device section formed on said substrate adjacent said photogate having a sensing node connected to said readout circuit and at least one charge coupled device stage capable of transferring charge from said underlying portion of the substrate to said sensing node,

15 an electronic shutter formed on said substrate adjacent said photogate and capable of draining charge from said underlying portion of the substrate.

38. The imaging device of Claim 37 wherein:

20 said sensing node of said charge coupled device section comprises a floating node; and

said charge coupled device stage comprises a transfer gate between said floating node and said photogate.

39. The imaging device of Claim 37, wherein each of said pixel cells further comprises:

a drain diffusion connected to a drain bias voltage; and

5 a reset gate between said sensing node and said drain diffusion.

40. The imaging device of Claim 39, wherein said electronic shutter comprises:

10 said drain diffusion; and

a shutter gate between said photogate and said drain diffusion.

41. The imaging device of Claim 37, wherein said electronic shutter comprises:

15 a shutter drain diffusion connected to a shutter drain bias voltage; and

a shutter gate between said photogate and said shutter drain diffusion.

20 42. The imaging device of Claim 41, wherein each one of said pixel cells further comprises:

a drain diffusion connected to a drain bias voltage; and

a reset gate between said floating node and said drain diffusion; and wherein,

the shutter drain diffusion is the drain diffusion of an adjacent pixel cell.

5

43. The imaging device of Claim 38, wherein:

said photogate is connected to a photogate bias voltage;

10 said transfer gate is connected to a transfer gate bias voltage;

said electronic shutter comprises,

a shutter drain diffusion connected to a shutter drain bias voltage, and

15 a shutter gate between said photogate and said shutter drain diffusion; and

in a closed shutter mode, where the shutter drain bias voltage is greater than the photogate bias voltage which is in turn greater than the transfer gate bias voltage, the electronic shutter drains charge from said  
20 underlying portion of the substrate.

44. The imaging device of Claim 43, wherein:

in an integrating mode, where the photogate bias voltage is greater than the shutter drain bias voltage,

charge accumulates in said underlying portion of said substrate.

45. The imaging device of Claim 44, wherein:

5           in the integrating mode, the shutter drain bias voltage is greater than the transfer gate bias voltage, thereby providing anti-blooming control.

46. The imaging device of Claim 44, wherein:

10           in a charge transfer mode, where the shutter drain bias voltage is smaller than the transfer gate bias voltage and the photogate bias voltage is pulsed to a smaller voltage than the transfer gate bias voltage, charge is transferred from said underlying portion of said substrate  
15           to said sensing node.

47. The imaging device of Claim 37, wherein a first gap exists between the photogate and the charge coupled device section and a second gap exists between the photogate  
20           and the electronic shutter, and wherein the photogate further comprises:

          a first overlying section which overlies the first gap; and,

          a second overlying section which overlies the  
25           second gap.

48. The imaging device of Claim 37, wherein a first gap exists between the photogate and the charge coupled device section and a second gap exists between the photogate and the electronic shutter, the imaging device further comprising:

a first floating diffusion underlying the first gap; and,

a second floating diffusion underlying the second gap.

49. An anti-blooming active pixel device, comprising:

a substrate;

a charge collecting area in said substrate, said charge collecting area including a controlling element which controls accumulation of charge in said charge collection area, according to an applied bias;

a charge sink area, separated from said charge collecting area;

a first transfer element, coupled between said charge collecting area and said charge sink area, said first transfer element transferring charge when biased to a level lower in potential than a potential of the bias on said controlling element;

wherein said first transfer element is biased to a first level to remove charge from said charge collecting

area, and biased to a second level to allow charge to collect in said charge collecting area, said second level being a level which is lower than a maximum level which would allow all charge to collect in said charge collecting area to prevent blooming.

50. A device as in claim 49 further comprising a floating element, a charge detection device, and a second transfer element connected between said light collecting area and said floating element, said second transfer element selectively biased between a first level which blocks charge in said charge collecting area from transferring to said floating element, and a second level which allows charge in said charge collecting area to transfer to said floating element, wherein a level of bias on said second transfer element is a higher potential than a level of bias on said transfer element while charge is being accumulated to prevent excess charge from spilling into said floating element.

51. A device as in claim 50, further comprising a charge storage area, coupled between said charge collecting area and said floating element.

52. A device as in claim 51, further comprising: a lens element layer, formed as a layer overlying at least a portion of said optically blocked layer, and which refracts light from said optically blocked layer to said optically unblocked layer.

53. A shuttered active pixel device, comprising:  
a light collection area which collects information indicative of light therein;  
a shuttering portion, which removes said information from said light area, and a floating node, which is sampled prior to charge transfer thereto and subsequent to charge transfer thereto, said floating node receiving charge from said collection area.

54. A method of operating an optical pixel cell device comprising:  
forming a substrate with an optical blocking layer located adjacent said substrate which divides said substrate into an optically blocked area and an optically unblocked area;  
accumulating charge in said optically unblocked area; and  
storing and processing charge in said optically blocked area.

55. A method of operating an active pixel sensor, comprising:

5 defining a beginning of an integration period and an end of an integration period during which integration period charge is to be accumulated;

10 accumulating charge in multiple photocollectors beginning at the beginning of the integration period to store incoming charge into a photogate well of multiple elements within the active pixel sensor;

at the end of the integration period, transferring accumulated charge from each said photocollector to an associated storage well;

15 sampling a value of a first floating node, associated with a first storage well, at a first time;

sampling a value of a second floating node, associated with a second storage well, at a second time subsequent to said first time; and

20 using said values obtained from said first and second floating nodes with one another, said values being correlated with one another and un smeared even though sampled at different times.



56. A method as in claim 55 further comprising providing an anti-blooming control during the integration period.

5        57. A method as in claim 55 wherein said anti-blooming control comprises biasing a first gate which is connected to a sink to a level lower than said first level.

10

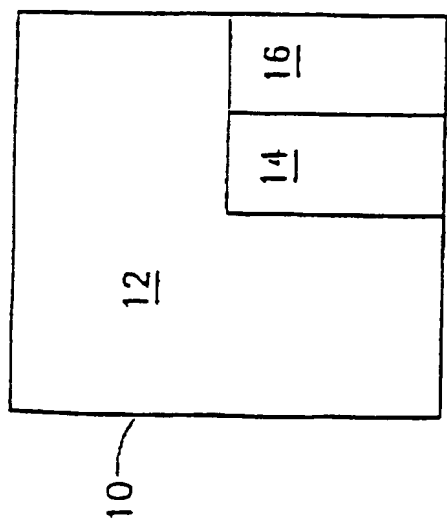


FIG. 1

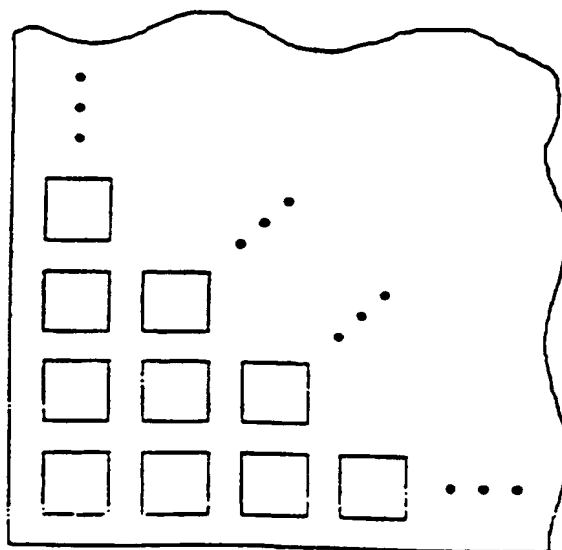


FIG. 2

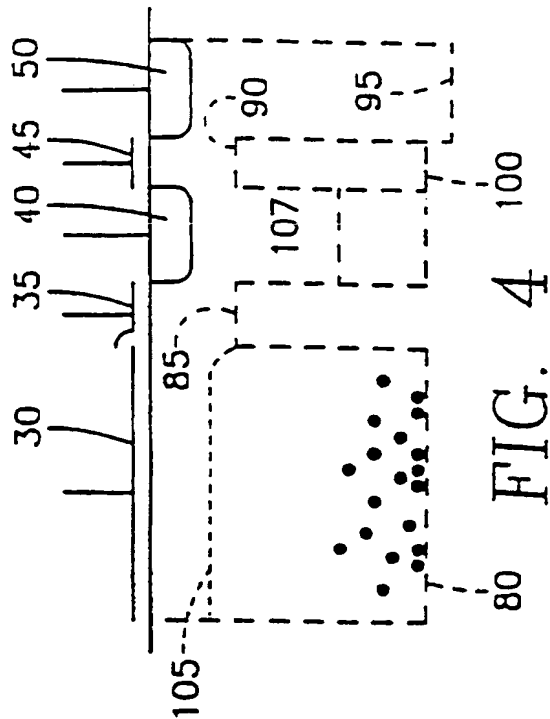


FIG. 4

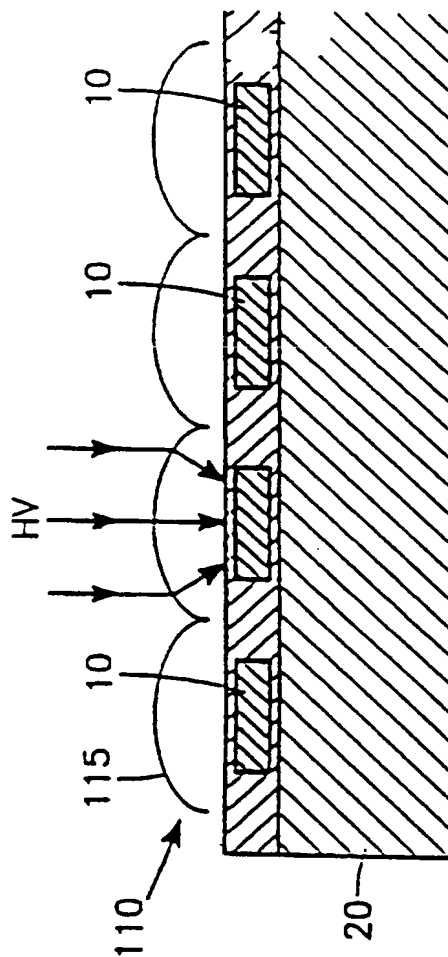


FIG. 5

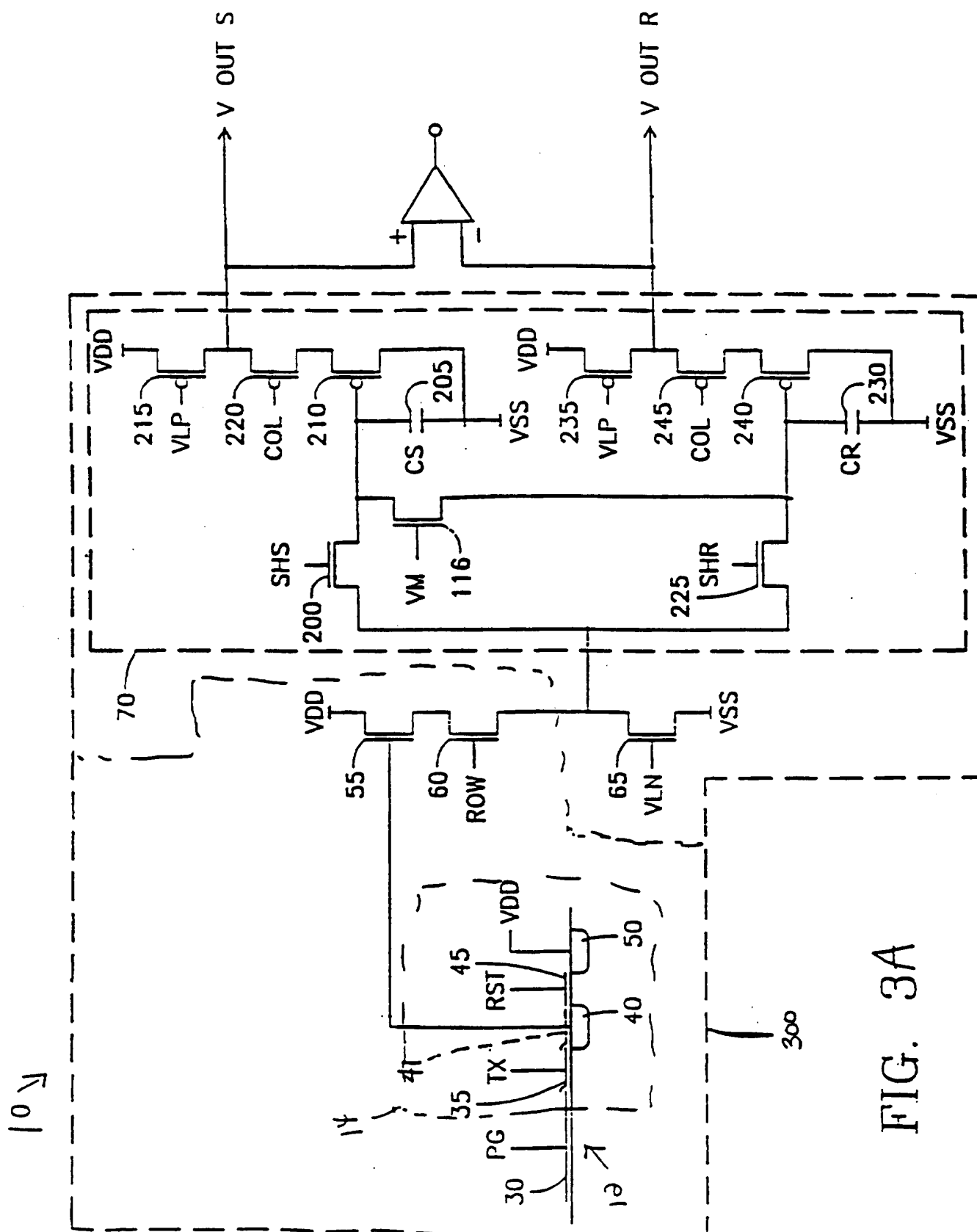
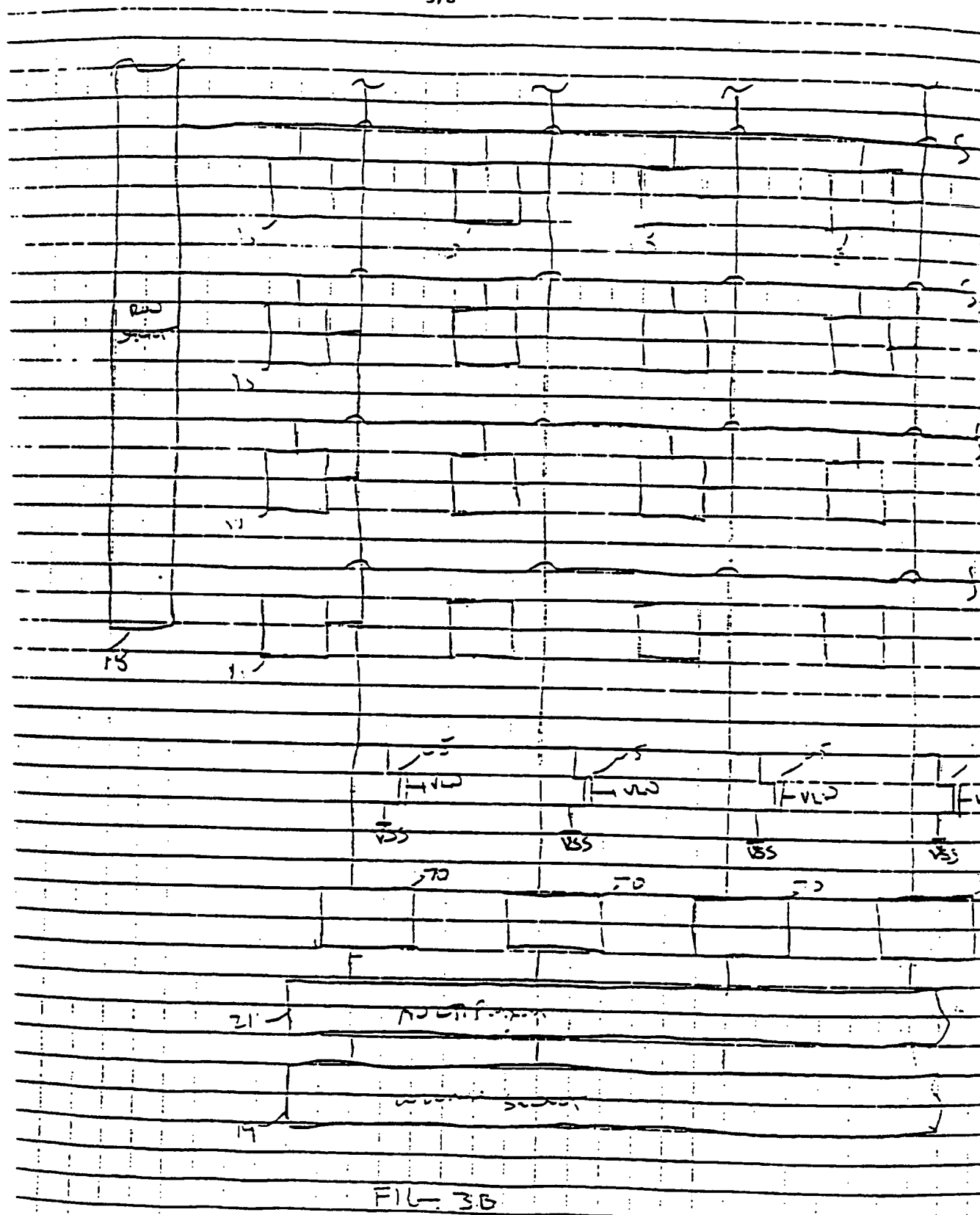
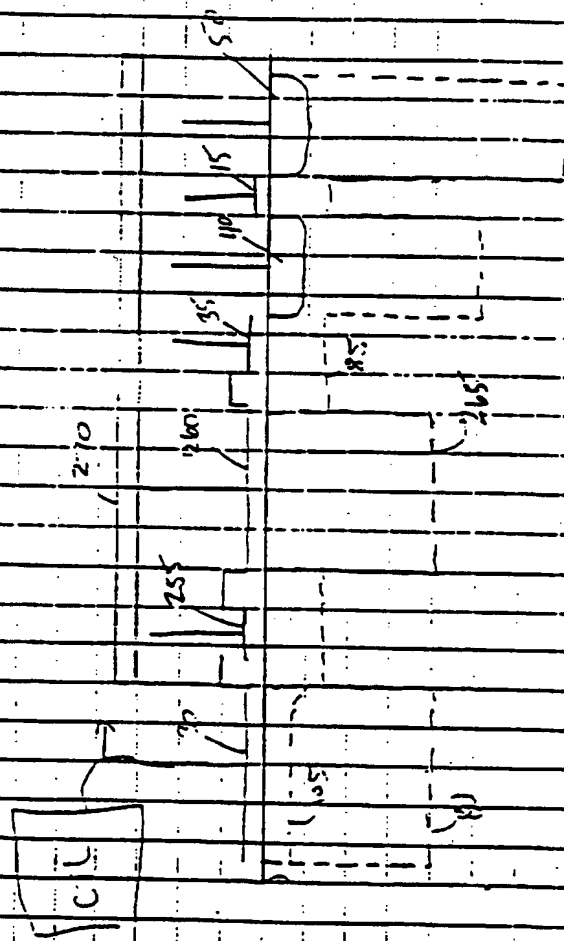


FIG. 3A

3/8



4/8



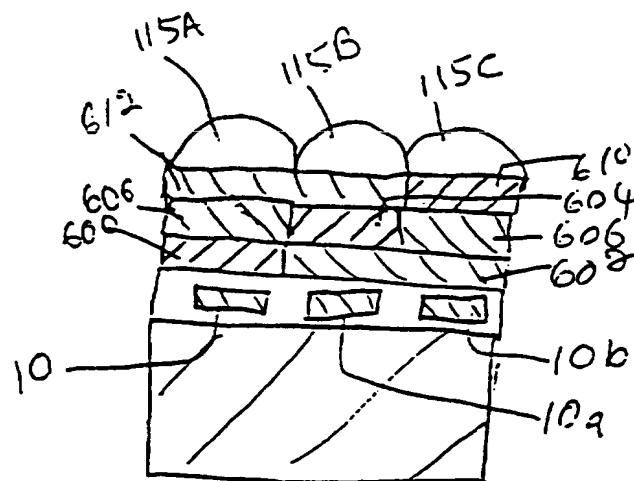


FIG 6A

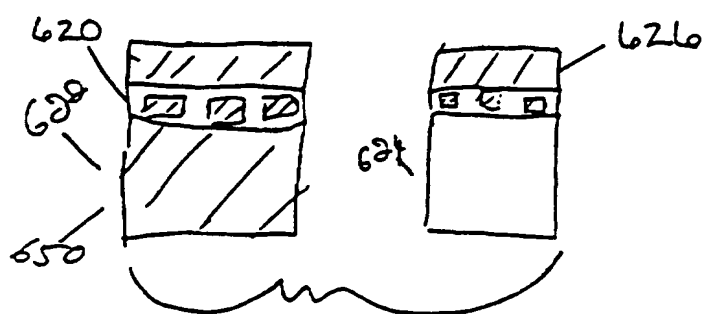


FIG 6B

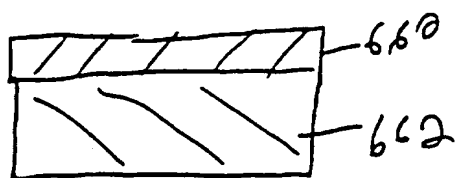
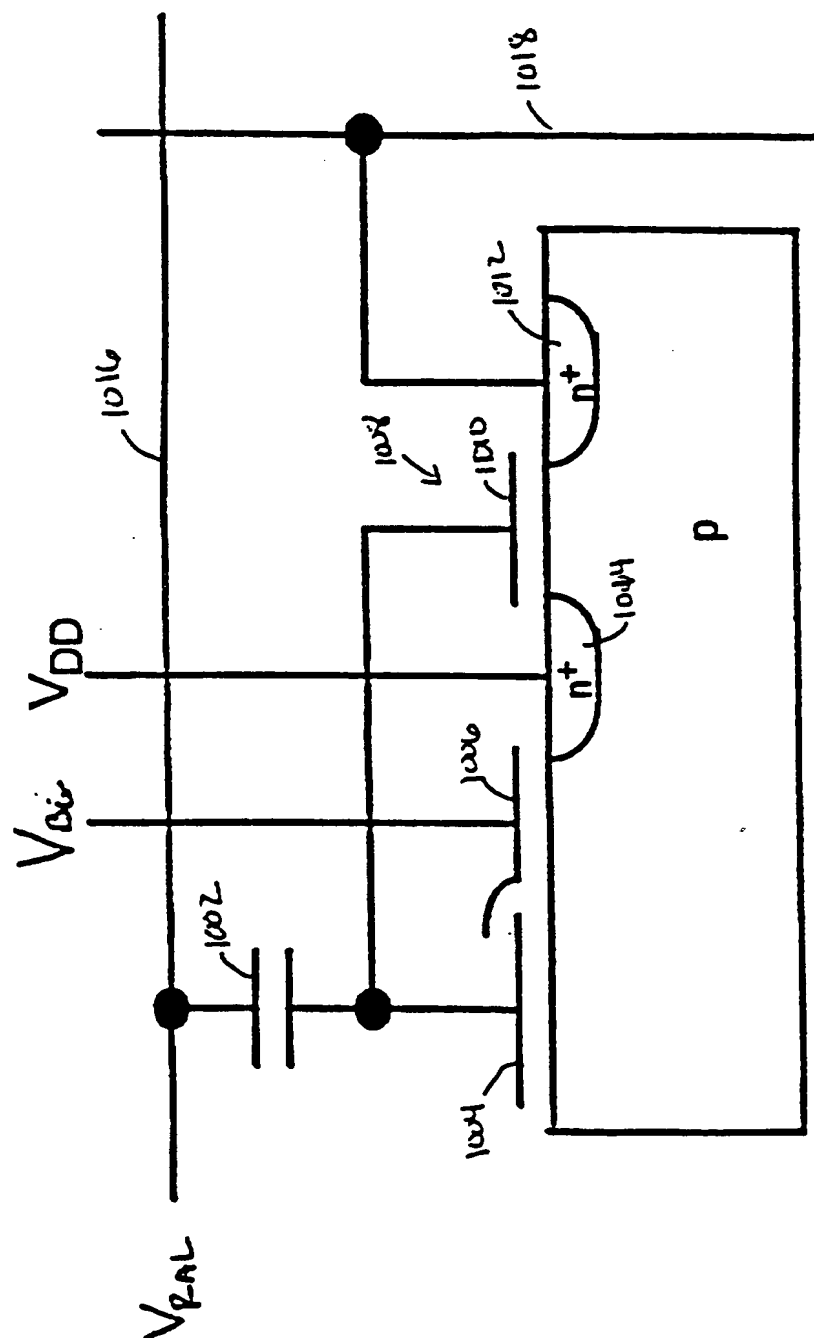


FIG 6 C





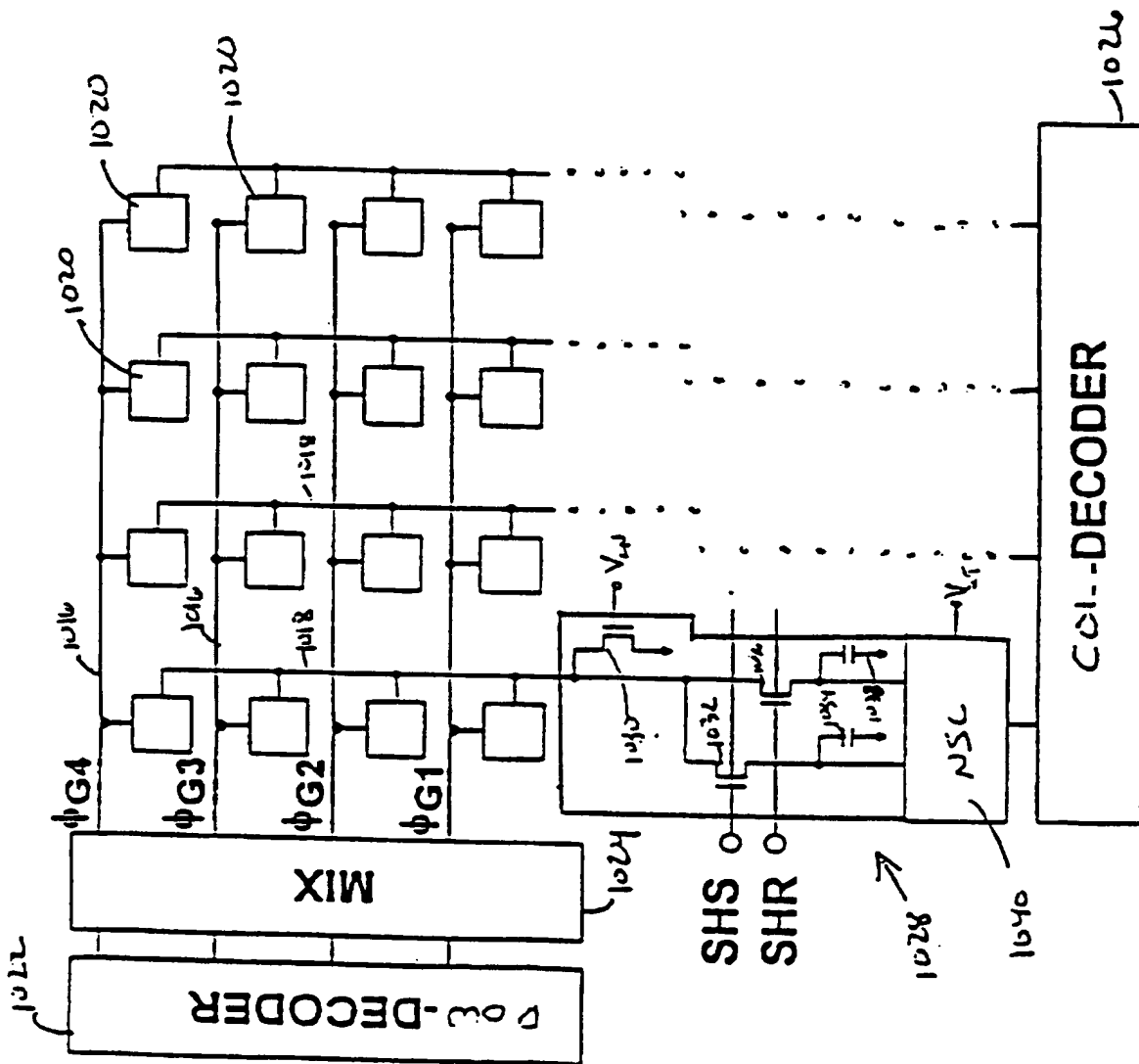


FIG. 7



(51) International Patent Classification <sup>6</sup> : <b>G11C 19/28</b>		<b>A3</b>	(11) International Publication Number: <b>WO 97/28558</b>
			(43) International Publication Date: 7 August 1997 (07.08.97)
(21) International Application Number: <b>PCT/US97/00927</b>		(74) Agent: HARRIS, Scott, C.; Fish & Richardson P.C., Suite 1400, 4225 Executive Square, La Jolla, CA 92037 (US).	
(22) International Filing Date: 22 January 1997 (22.01.97)			
(30) Priority Data:		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
60/010,305 22 January 1996 (22.01.96) US			
60/013,700 20 March 1996 (20.03.96) US			
(60) Parent Applications or Grants			
(63) Related by Continuation			
US 60/013,700 (CON)			
Filed on 20 March 1996 (20.03.96)			
US 60/010,305 (CON)			
Filed on 22 January 1996 (22.01.96)			
(71) Applicant (for all designated States except US): CALIFORNIA INSTITUTE OF TECHNOLOGY [US/US]; 1201 East California Boulevard, Pasadena, CA 91125 (US).		Published With international search report.	
(72) Inventor; and		(88) Date of publication of the international search report: 2 October 1997 (02.10.97)	
(75) Inventor/Applicant (for US only): FOSSUM, Eric, R. [US/US]; Photobit, Suite 104, 2529 Foothill Boulevard, La Crescenta, CA 91214 (US).			

Hand-drawn cross-section diagram of a dam on grid paper. The dam has a crest width of 2.70m and a height of 7.0m. The upstream face is on the left, and the downstream face is on the right. The downstream slope is divided into three sections with angles of 25°, 35°, and 40°. The base of the dam is 26.5m wide. The downstream toe is 5.7m from the right edge of the grid. The dam is labeled 'C-1' in a box on the left. The grid lines are numbered 1 through 10 along the top and bottom edges.

An active pixel cell includes electronic shuttering capability. The cell can be "shuttered" to prevent additional charge accumulation. One mode transfers the current charge to a storage node (260) that is blocked against accumulation of optical radiation. The charge is sampled from a floating node (40). Since the charge is stored, the node (40) can be sampled at the beginning and the end of every cycle. Another aspect allows charge to spill out of the well whenever the charge amount gets higher than some amount, thereby providing anti blooming.

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgyzstan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	KZ	Kazakhstan	SG	Singapore
CH	Switzerland	LI	Liechtenstein	SI	Slovenia
CI	Côte d'Ivoire	LK	Sri Lanka	SK	Slovakia
CM	Cameroon	LR	Liberia	SN	Senegal
CN	China	LT	Lithuania	SZ	Swaziland
CS	Czechoslovakia	LU	Luxembourg	TD	Chad
CZ	Czech Republic	LV	Latvia	TG	Togo
DE	Germany	MC	Monaco	TJ	Tajikistan
DK	Denmark	MD	Republic of Moldova	TT	Trinidad and Tobago
EE	Estonia	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	UG	Uganda
FI	Finland	MN	Mongolia	US	United States of America
FR	France	MR	Mauritania	UZ	Uzbekistan
GA	Gabon			VN	Viet Nam

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US97/00927

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G11C 19/28

US CL : 377/60

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 377/60;257/239,292,294

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,5,471,515 A (FOSSUM ET AL) 28 November 1995 (28/11/95), see figures 1,3,5.	1, 4 - 10, 12, 13, 16, 18, 20,21,23 24,53,55
Y,E	US 5,631,704 A (DICKERSON ET AL) 20 MAY 1997 (20/05/97), SEE FIGURES 1,2.	1,4,5,8-10, 13,16,24, 53-55
Y,P	US 5,563,429 A (ISOGAI) 08 OCTOBER 1996 (08/10/96), SEE FIGURE 1A,1B.	1,8,20,53, 54
Y	JP 5-235317 A (ISOGAI) 10 SEPTEMBER 1993 (10/09/93) SEE ABSTRACT, FIGURE 1(A),1(B).	1,8,20,53, 54

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*A* document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*E* earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Z* document member of the same patent family
*O* document referring to an oral disclosure, use, exhibition or other means	
*P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

11 JUNE 1997

Date of mailing of the international search report

24 JUL 1997

Name and mailing address of the ISA/US  
Commissioner of Patents and Trademarks  
Box PCT  
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

GENE M. MUNSON

Telephone No. (703) 308-4925

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US97/00927

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,155,094 A (OHBA ET AL) 15 MAY 1997 (15/05/79) SEE FIGURE 2B.	1,8,20,53, 54
Y	US 4,093,872 A (HARTMAN ET AL) 06 JUNE 1978 (06/06/78), SEE FIGURES 1-3.	1,8,20,53, 54
Y	US 4,980,735 A (YAMAWAKI) 25 DECEMBER 1990 (25/12/90), SEE FIGURES 1,2,5.	1-3,6,14, 15,17,18, 21, 24,27,51, 55
Y	US 5,051,797 A (ERHARDT) 24 SEPTEMBER 1991 (24/09/91), SEE FIGURES 1-3.	1-3,11,14, 17,19,21, 22,24-33, 45,49-51, 56,57
A	US 5,323,052 A (KOYAMA) 21 JUNE 1995 (21/06/94), SEE FIGURES 5,6,7.	7,12
A	US 4,287,441 A (SMITH) 01 SEPTEMBER 1981 (01/09/81), SEE FIGURE 8.	13,24,55
A	US 4,683,580 A (MATSUNAGA) 28 JULY 1987 (28/07/87), SEE FIGURES 1,5.	13,24,55

Form PCT/ISA/210 (continuation of second sheet)(July 1992)\*